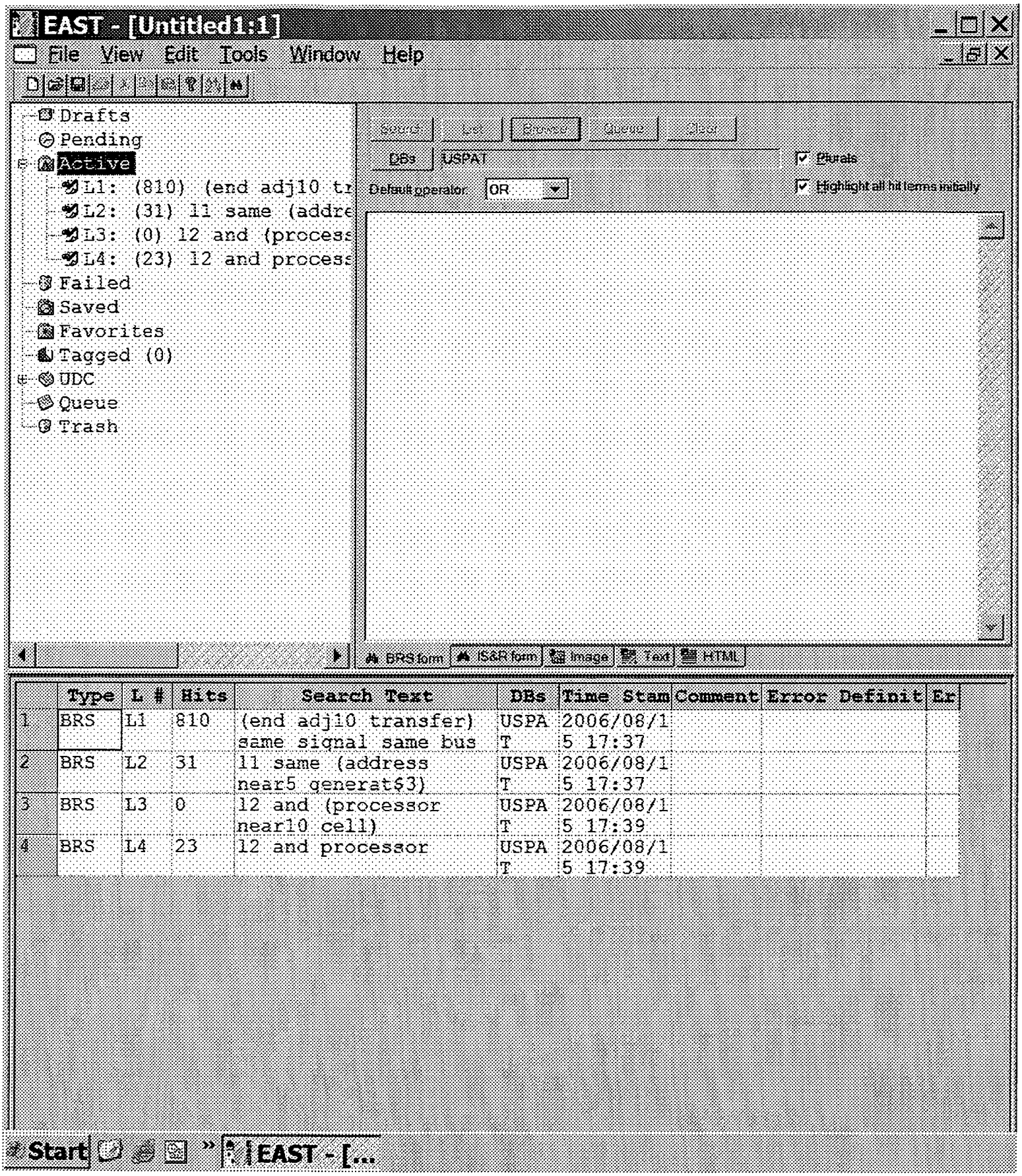
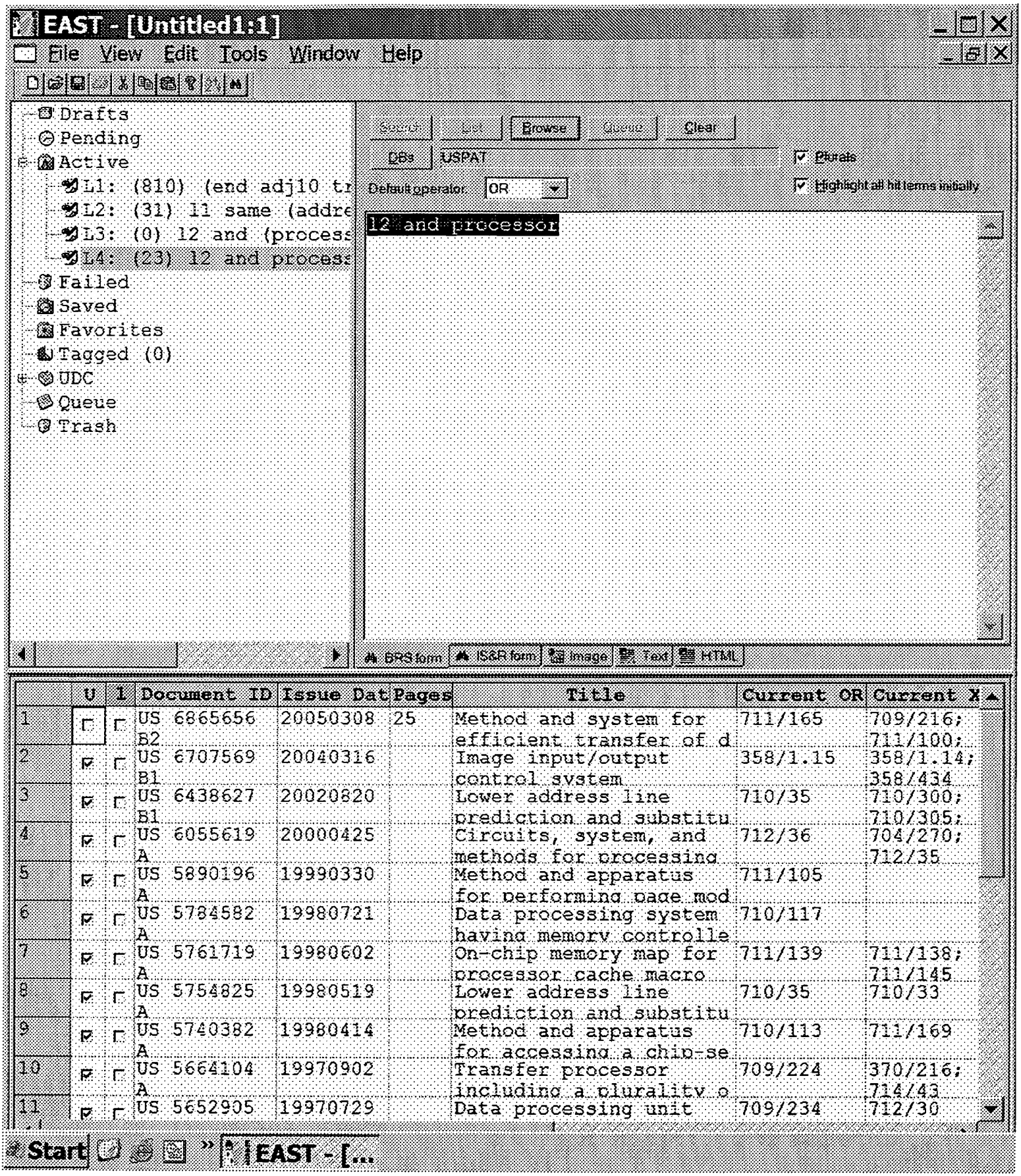
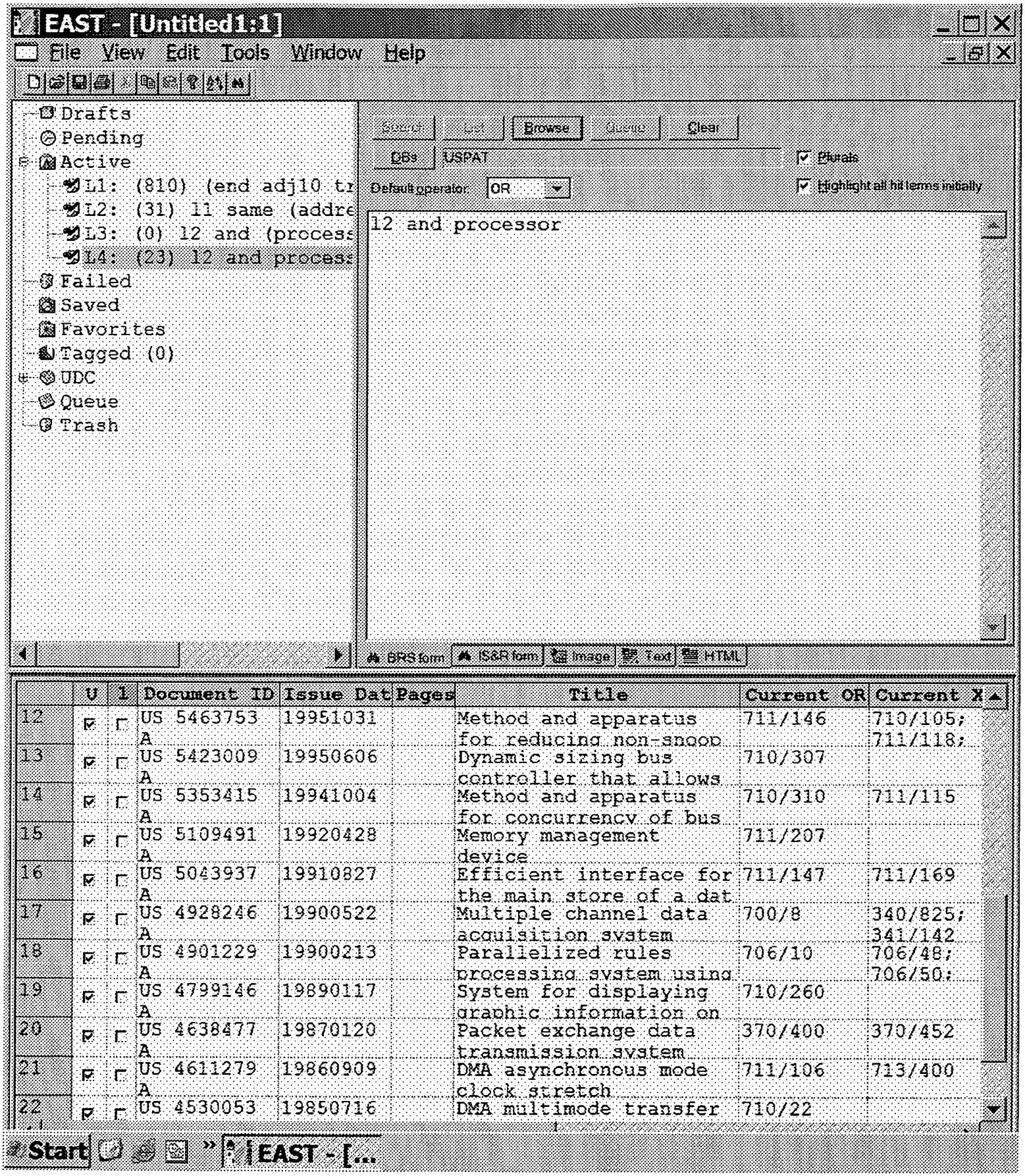



| | Type | L # | Hits | Search Text | DBs | Time Stam | Comment | Error Definit | Er |
|---|---|---|---|---|---|---|---|---|---|
| 1 | BRS | L1 | 810 | (end adj10 transfer) same signal same bus | USPAT | 2006/08/15 17:37 | | | |
| 2 | BRS | L2 | 31 | 11 same (address near5 generat$3) | USPAT | 2006/08/15 17:37 | | | |
| 3 | BRS | L3 | 0 | 12 and (processor near10 cell) | USPAT | 2006/08/15 17:39 | | | |
| 4 | BRS | L4 | 23 | 12 and processor | USPAT | 2006/08/15 17:39 | | | |




| | U | 1 | Document ID | Issue Dat | Pages | Title | Current OR | Current X |
|---|---|---|---|---|---|---|---|---|
| 1 | ☐ | ☐ | US 6865656 B2 | 20050308 | 25 | Method and system for efficient transfer of d | 711/165 | 709/216; 711/100; |
| 2 | ☑ | ☐ | US 6707569 B1 | 20040316 | | Image input/output control system | 358/1.15 | 358/1.14; 358/434 |
| 3 | ☑ | ☐ | US 6438627 B1 | 20020820 | | Lower address line prediction and substitu | 710/35 | 710/300; 710/305; |
| 4 | ☑ | ☐ | US 6055619 A | 20000425 | | Circuits, system, and methods for processing | 712/36 | 704/270; 712/35 |
| 5 | ☑ | ☐ | US 5890196 A | 19990330 | | Method and apparatus for performing page mod | 711/105 | |
| 6 | ☑ | ☐ | US 5784582 A | 19980721 | | Data processing system having memory controlle | 710/117 | |
| 7 | ☑ | ☐ | US 5761719 A | 19980602 | | On-chip memory map for processor cache macro | 711/139 | 711/138; 711/145 |
| 8 | ☑ | ☐ | US 5754825 A | 19980519 | | Lower address line prediction and substitu | 710/35 | 710/33 |
| 9 | ☑ | ☐ | US 5740382 A | 19980414 | | Method and apparatus for accessing a chip-se | 710/113 | 711/169 |
| 10 | ☑ | ☐ | US 5664104 A | 19970902 | | Transfer processor including a plurality o | 709/224 | 370/216; 714/43 |
| 11 | ☑ | ☐ | US 5652905 | 19970729 | | Data processing unit | 709/234 | 712/30 |


EAST - [Untitled1:1]
File View Edit Tools Window Help
Drafts
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L1: (810) (end adj10 tr
L2: (31) 11 same (addre
L3: (0) 12 and (process
L4: (23) 12 and process
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OR
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Title
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12 US 5463753 A 19951031 Method and apparatus for reducing non-snoop 711/146 710/105; 711/118;
13 US 5423009 A 19950606 Dynamic sizing bus controller that allows 710/307
14 US 5353415 A 19941004 Method and apparatus for concurrency of bus 710/310 711/115
15 US 5109491 A 19920428 Memory management device 711/207
16 US 5043937 A 19910827 Efficient interface for the main store of a dat 711/147 711/169
17 US 4928246 A 19900522 Multiple channel data acquisition system 700/8 340/825; 341/142
18 US 4901229 A 19900213 Parallelized rules processing system using 706/10 706/48; 706/50;
19 US 4799146 A 19890117 System for displaying graphic information on 710/260
20 US 4638477 A 19870120 Packet exchange data transmission system 370/400 370/452
21 US 4611279 A 19860909 DMA asynchronous mode clock stretch 711/106 713/400
22 US 4530053 19850716 DMA multimode transfer 710/22
Start
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